**Power Optimization of Linear Feedback Shift Register (LFSR) for Low Power BIST implemented in HDL**

ABSTRACT:

LFSR based Pseudo random test pattern generator is used in the testing of ASIC chips which generates random sequences of test patterns. This project deals with the design of LFSR and also how to multiplex the Test inputs with the ASIC inputs to reduce the additional test input pins required for the ASIC. This project presents a novel low-transition Linear Feedback Shift Register (LFSR) that is based on some new observations about the output sequence of a conventional LFSR. The proposed design, called bit-swapping LFSR (BS-LFSR), is composed of an LFSR and a 2 × 1 multiplexer. When used to generate test patterns for scan-based built-in self-tests, it reduces the number of transitions that occur at the scan-chain input during scan shift operation by 50% when compared to those patterns produced by a conventional LFSR. Hence, it reduces the overall switching activity in the circuit under test during test applications. The BS-LFSR is combined with a scan-chain-ordering algorithm that orders the cells in a way that reduces the average and peak power (scan and capture) in the test cycle or while scanning out a response to a signature analyzer. These techniques have a substantial effect on average- and peak power reductions with negligible effect on fault coverage or test application time. Experimental results on ISCAS’89 benchmark circuits show up to 65% and 55% reductions in average and peak power, respectively. Index Terms Built-in self-test (BIST), linear feedback shift register (LFSR), low-power test, pseudorandom pattern generator, scanchain ordering, weighted switching activity (WSA).

**LANGUAGE USED:**

**TOOLS REQUIRED:**

* MODELSIM – Simulation
* XILINX-ISE – Synthesis